ABSTRACT OF THE DISCLOSURE

A memory cell is formed for a memory cell array that is comprised of a plurality of the memory cells arranged in rows and columns. Deep trenches having sidewalls is formed within a semiconductor substrate. A buried plate region adjoining a deep trench is formed within the semiconductor substrate, and a dielectric film is formed along the sidewalls of the deep trench. A masking layer is patterned such that a portion of the dielectric film is covered by the masking layer and a remaining portion of the dielectric film is exposed. An upper region of the exposed portion of the dielectric film is removed such that a trench collar is formed along a middle portion of a side of the deep trench. The deep trench is partly filled with doped polysilicon. The dopants in the polysilicon diffuse through the side of the deep trench into adjoining regions of the semiconductor substrate during subsequent thermal processing steps to form a buried strap region along a side of the deep trench. The semiconductor substrate is patterned and etched to form at least one isolation trench that adjoins the isolation trench and two of the deep trenches and includes a buried strap region. The patterning uses a mask comprised of a lines and spaces pattern such that at least one active area is defined by the isolation trench and by the deep trench. Each of the lines and the spaces extends across the memory cell array.